REMARKS

Claims 1-9 were pending in the application. Claims 4-6, 8 and 9 were withdrawn from consideration pursuant to a restriction requirement. Claims 1-3 and 7 were rejected under 35 U.S.C. 102 over Takeuchi (U.S. patent no. 5,661,056). Claims 2-4, 8, 9 are canceled, and Claims 10-29 are added.

Claims 1-3, 10-16. Claim 1 is amended to recite "ion implantation of a material comprising nitrogen into the silicon surface". Takeuchi does not teach or suggest ion implantation. See for example Takeuchi, col. 4, line 17 ("CVD") or line 25 ("Rapid Thermal Nitrization").

Claims 2-3 and 10 depend from Claim 1.

Claim 11 depends from Claim 10, and further recites "ion implantation of a material comprising nitrogen into the silicon oxide surface". Takeuchi does not teach or suggest ion implantation into a silicon oxide surface as in Claim 10.

Claim 12 depends from Claim 10.

Claim 13 depends from Claim 10 and further recites "remote plasma nitridation". Claim 14 depends from Claim 10 and further recites "decoupled plasma nitridation". Takeuchi does not teach or suggest using these techniques.

Claim 15 depends from Claim 10, and further recites "a nitrided silicon oxide layer less than 3 nm thick". Takeuchi discloses an 8 nm thickness (col. 7, line 11), and states that a large thickness is desirable (col. 8, lines 19-20).

Similar reasons apply to Claim 16.

Claims 7, 29. Claim 7 recites "ion implantation of a material comprising nitrogen" into a surface comprising silicon oxide. Takeuchi does not teach or suggest this feature.

Claim 29 depends from Claim 7, and further recites a less than 3 nm thickness. See the discussion above in connection with Claim 15.

Claims 17-28. Claim 17 recites "remote plasma nitridation and/or decoupled plasma nitridation". Takeuchi does not teach or suggest these techniques.

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Claims 18-22 depend from Claim 17.

Claim 23 also depends from Claim 17, and further recites "ion implantation of a material comprising nitrogen into the silicon oxide surface". See the discussion above in connection with Claim 11.

With regard to Claims 25, 26, see the discussion above in connection with Claims 13, 14.

With regard to Claims 27, 28, see the discussion above in connection with Claims 15, 16.

Questions regarding this case can be addressed by contacting the undersigned by email or telephone at the address or phone number below.

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Version with Markings to Show Changes Made

IN THE SPECIFICATION

Please amend the paragraph on page 3, lines 11-18, as follows:

Fig. 2 illustrates a cross section of a nonvolatile memory cell at an early stage of fabrication. Semiconductor substrate 120 (monocrystalline silicon or some other material) is processed to form a suitably doped channel region 150 (type P in Fig. 2, but an N type channel can also be used). Dielectric 130 is formed on substrate 120 over channel 150. Dielectric 130 may be thermally grown silicon dioxide or some other type of dielectric. Then polysilicon layer 110 is deposited and doped during or after deposition. See for example U.S. patent application 09/640,139 filed August 15, 2000 and incorporated herein by reference **(now U.S. patent no. 6,355,524 issued March 12, 2002)**.

Please amend the paragraph on page 5, lines 12-22, as follows:

Known techniques can be used to complete the memory fabrication. In the example of Fig. 4, silicon nitride layer 410 is formed by low pressure CVD (LPCVD) on layer 310. Silicon dioxide 420 is deposited by CVD, or thermally grown, on layer 410. Layers 310, 410, 420 are referenced as 160. Doped polysilicon 170, or some other conductive material, is deposited to provide the control gates (possibly wordlines each of which provides the control gates for a row of memory cells). The layers 170, 420, 410, 310, 110, 130 are patterned as needed. Source/drain regions 140 are formed by doping. Additional layers (not shown) may be formed to provide select gates, erase gates, or other features. See the aforementioned U.S. patent **no. 6,355,524 [application 09/640,139]** for an exemplary memory fabrication process that can be modified to incorporate the floating gate nitridation described above.

IN THE CLAIMS

1. (Amended) A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

forming a first layer comprising **a** silicon **surface**, the first layer being to provide one or more floating gates for the nonvolatile memory;

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nitriding [a] **the silicon** surface of the first layer to incorporate nitrogen atoms into said surface**, wherein the nitriding operation comprises ion implantation of a material comprising nitrogen into the silicon surface**;

forming a first dielectric at the nitrided surface, wherein forming the first dielectric comprises forming silicon oxide at the nitrided surface;

forming a conductive layer separated from the nitrided surface by the first dielectric, the conductive layer providing one or more control gates for the nonvolatile memory.

2. (Unchanged) The method of Claim 1 wherein forming the silicon oxide at the nitrided surface comprises forming the silicon oxide by thermal oxidation.

3. (Amended) The method of Claim 1 wherein the **silicon** surface of the first layer is a polysilicon surface.

Please cancel Claims 4-6.

7. (Amended) A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

forming a first layer to provide one or more floating gates for the nonvolatile memory;

forming a first dielectric on a surface of the first layer, wherein the first dielectric comprises a first surface comprising silicon oxide;

nitriding the first surface of the first dielectric to incorporate nitrogen atoms into the first surface**, wherein the nitriding operation comprises ion implantation of a material comprising nitrogen into the first surface**;

forming a conductive layer on the nitrided first surface of the first dielectric, the conductive layer providing one or more control gates for the nonvolatile memory.

Please cancel Claims 8 and 9.

Please add the following claims.

10. (New) The method of Claim 1 wherein forming the first dielectric comprises:

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forming the first dielectric to have a silicon oxide surface; and

nitriding the silicon oxide surface of the first dielectric to incorporate nitrogen atoms into the silicon oxide surface.

11. (New) The method of Claim 10 wherein the nitriding of the silicon oxide surface comprises ion implantation of a material comprising nitrogen into the silicon oxide surface.

12. (New) The method of Claim 10 wherein the nitriding of the silicon oxide surface comprises generating a plasma comprising ions comprising nitrogen, and exposing the silicon oxide surface to the plasma.

13. (New) The method of Claim 10 wherein the nitriding of the silicon oxide surface comprises remote plasma nitridation.

14. (New) The method of Claim 10 wherein the nitriding of the silicon oxide surface comprises decoupled plasma nitridation.

15. (New) The method of Claim 10 wherein the nitriding of the silicon oxide surface results in forming at the silicon oxide surface a nitrided silicon oxide layer less than 3 nm thick.

16. (New) The method of Claim 1 wherein the nitriding of the silicon surface results in forming at the silicon surface a layer of nitrided silicon less than 3 nm thick.

17. (New) A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

forming a first layer comprising a silicon surface, the first layer being to provide one or more floating gates for the nonvolatile memory;

nitriding the silicon surface of the first layer by remote plasma nitridation and/or decoupled plasma nitridation to incorporate nitrogen atoms into said surface;

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forming a first dielectric at the nitrided surface, wherein forming the first dielectric comprises forming silicon oxide at the nitrided surface;

forming a conductive layer separated from the nitrided surface by the first dielectric, the conductive layer providing one or more control gates for the nonvolatile memory.

18. (New) The method of Claim 17 wherein the nitriding operation comprises remote plasma nitridation.

19. (New) The method of Claim 17 wherein the nitriding operation comprises decoupled plasma nitridation.

20. (New) The method of Claim 17 wherein forming the silicon oxide at the nitrided surface comprises forming the silicon oxide by thermal oxidation.

21. (New) The method of Claim 17 wherein the silicon surface of the first layer is a polysilicon surface.

22. (New) The method of Claim 17 wherein forming the first dielectric comprises:

forming the first dielectric to have a silicon oxide surface; and

nitriding the silicon oxide surface of the first dielectric to incorporate nitrogen atoms into the silicon oxide surface.

23. (New) The method of Claim 22 wherein the nitriding of the silicon oxide surface comprises ion implantation of a material comprising nitrogen into the silicon oxide surface.

24. (New) The method of Claim 22 wherein the nitriding of the silicon oxide surface comprises generating a plasma comprising ions comprising nitrogen, and exposing the silicon oxide surface to the plasma.

25. (New) The method of Claim 22 wherein the nitriding of the silicon oxide surface comprises remote plasma nitridation.

26. (New) The method of Claim 22 wherein the nitriding of the silicon oxide surface comprises decoupled plasma nitridation.

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27. (New) The method of Claim 22 wherein the nitriding of the silicon oxide surface results in forming at the silicon oxide surface a nitrided silicon oxide layer less than 3 nm thick.

28. (New) The method of Claim 17 wherein the nitriding of the silicon surface results in forming at the silicon surface a layer of nitrided silicon less than 3 nm thick.

29. (New) The method of Claim 7 wherein the ion implantation results in forming at the first surface a nitrided silicon oxide layer less than 3 nm thick.

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